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Amendments to the Claim of Priority:

Please add the following new heading and paragraph on page 1 before the heading "BACKGROUND".

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of Application No. 10/114,375, filed April 1, 2002.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An impedance network, comprising:
 - a plurality of impedance elements;
 - at least one end terminal;
 - a first plurality of switching elements selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of impedance elements in the plurality of impedance elements;
 - a wiper terminal; and
 - a second plurality of switching elements selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of impedance elements in the plurality of impedance elements.
2. (Original) The network of claim 1, wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.
3. (Original) The network of claim 1, wherein the second plurality of switching elements is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.
4. (Original) The network of claim 1, wherein the first specified increment is four impedance elements.
5. (Original) The network of claim 1, wherein the second specified increment is one impedance element.

6. (Original) The network of claim 1, wherein said first plurality of switching elements includes a plurality of transistors.

7. (Currently Amended) The network of claim [[1]] 6, wherein said plurality of transistors includes a plurality of field-effect transistors (FET).

8. (Original) The network of claim 1, wherein said second plurality of switching elements includes a plurality of transistors.

Claims 9-11 (Canceled)

12. (Original) A resistor network having a plurality of resistors, comprising:
at least one end terminal;
a wiper terminal;
a first plurality of switching elements selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of resistors in the network; and
a second plurality of switching elements selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of resistors in the network.

13. (Original) The network of claim 12, wherein said first set of switching elements includes a plurality of transistors.

14. (Original) The network of claim 13, wherein said plurality of transistors includes a plurality of field-effect transistors (FET).

15. (Original) A method for configuring an impedance network, comprising:
providing a plurality of impedance elements;
providing at least one end terminal and a wiper terminal;
first selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of impedance elements in the network; and

second selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of impedance elements in the network.

16. (Original) The method of claim 15, wherein the first and second selectively providing includes selecting the first specified increment to be larger than the second specified increment.

17. (Original) The method of claim 15, wherein the first selectively providing includes providing coarse adjustment.

18. (Original) The method of claim 15, wherein the second selectively providing includes providing fine adjustment.

19. (Canceled)

20. (Original) A method for configuring an impedance network, comprising: selectively connecting a first plurality of resistors to the two end terminals of a variable impedance network for coarse adjustment; selectively connecting a second plurality of resistors to the wiper terminal for fine adjustment; and configuring the first and second pluralities of resistors to provide all increments of resistance values.

21. (New) An impedance network, comprising:
first and second pluralities of impedance elements, each connected in series, one end of the series connection of the first plurality of impedance elements being connected to one end of the series connection of the second plurality of impedance elements;

a first end terminal connected to a second end of the first series connection of the first plurality of impedance elements;

a first plurality of switching elements selectively coupling nodes between impedances in the first plurality of impedance elements to the at least one end terminal, selectable at a first specified increment of impedance elements in the first plurality of impedance elements;

a wiper terminal; and

a second plurality of switching elements selectively coupling nodes between impedances in the second plurality of impedance elements to the wiper terminal, selectable at a second specified increment of impedance elements.

22. (New) The network of claim 21, wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

23. (New) The network of claim 21, further comprising:

a third plurality of impedance elements, each equal in number and value to the first plurality of impedance elements, each connected in series, one end of the series connection of the third plurality of impedance elements being connected to a second end of the series connection of the second plurality of impedance elements;

a second end terminal connected to a second end of the series connection of the third plurality of impedance elements; and

a third plurality of switching elements selectively coupling nodes between impedances in the third plurality of impedance elements to the second end terminal, selectable at a first specified increment of impedance elements in the third plurality of impedance elements;

wherein the second plurality of switching elements is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.

24. (New) The network on claim 23 further comprising:

fourth and fifth pluralities of impedance elements, each being equal in number and impedance to the number and impedance of the impedances in the second plurality of impedance elements;

the fourth plurality of impedance elements being coupled in series with one end coupled to the first terminal of the network of claim 23 and a second end coupled to a third terminal;

the fifth plurality of impedance elements being coupled in series with one end coupled to the second terminal of the network of claim 23 and a second end coupled to a fourth terminal;

a fourth plurality of switching elements selectively coupling nodes between impedances in the fourth plurality of impedance elements to the wiper terminal, selectable at the second specified increment of impedance elements in the fourth plurality of impedance elements; and

a fifth plurality of switching elements selectively coupling nodes between impedances in the fifth plurality of impedance elements to the wiper terminal, selectable at the second specified increment of impedance elements in the fifth plurality of impedance elements.

25. (New) The network of claim 24, wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

26. (New) The network of claim 24 wherein the impedance elements are resistances.

27. (New) The network of claim 21, wherein the first specified increment is four impedance elements.

28. (New) The network of claim 27, wherein the second specified increment is one impedance element.

29. (New) The network of claim 21, wherein said switching elements includes a plurality of transistors.

30. (New) The network of claim 29, wherein said plurality of transistors includes a plurality of field-effect transistors (FET).

31. (New) The network of claim 21 wherein the impedance elements are resistances.

32. (New) The network of claim 31 wherein the resistances at each end of the second plurality of resistances are reduced in resistance from the remaining resistances on the second plurality of resistances to compensate for switching element resistances.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Figs. 2B, 2C and 4. These sheets, which include Figs. 2B, 2C and 4 only, replace the original sheets including the same Figures.

In Fig. 2B, reference numerals 400, 402, 404 and 406 have been changed to 200, 202, 204 and 206, respectively.

In Fig. 2C, reference numerals 410, 412, 414, 416 and 418 have been changed to 210, 212, 214, 216 and 218, respectively.

In Fig. 4, the missing reference R has been added to one of the resistors.

Attachment: Annotated Sheets Showing Changes